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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,065	09/26/2006	Ryouichi Takeuchi	Q80875	8882

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EXAMINER	
WEBB, VERNON P	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,065	TAKEUCHI ET AL.	
	Examiner	Art Unit	
	VERNON P. WEBB	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *9-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-8,12 and 13* is/are rejected.

7)☐ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/04/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Application

1. This office action is in response to the filing of the amendment on 04 May 2009, Claims 1-15 are pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

3. Acknowledgement is made that the information disclosure statements filed on 05/04/2009 has been received and considered by the examiner. If the applicant is aware of any prior art or any other co-pending applications not already of record, he/she is reminded of his/her duty under 37 CFR 1.56 to disclose the same.

Allowable Subject Matter

4. Claims 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1, 2, and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoguchi et al. (U.S. Pub. Application 2006/0094140 A1) and further in view of Udagawa (U.S. Pub. Application 2003/0160253 A1).

8. Regarding claim 1, Inoguchi et al. discloses a pn-junction compound semiconductor light-emitting device comprising:

- a stacked structure (items 2-7 and 16-18, 20 and 21) including a light-emitting part composed of aluminum gallium indium phosphide (item 5), said light-emitting part comprising a light-emitting layer (item item7), a lower clad layer (item 6) and an upper clad layer (item 17) and a light-permeable substrate (item 1) for supporting the stacked structure (items 2-7 and 16-18, 20 and 21) (pg. 2, paragraphs [0021-0024] and [0031]; Figs. 1-3).

9. Inoguchi et al. does not disclose a pn-junction compound semiconductor light-emitting device, comprising a stacked structure including a conductive boron containing Group III-V compound semiconductor layer formed on the light-emitting part, and

wherein the light permeable substrate is joined to the stacked structure through the boron containing Group III-V compound semiconductor layer.

10. However Udagawa discloses a pn-junction compound semiconductor light-emitting device comprising a stacked structure (items 102-106) including a conductive boron containing Group III-V compound semiconductor layer (item 103) formed on the light-emitting part (item 104), and wherein the light permeable substrate (item 101) is joined to the stacked structure (items 102-106) through the boron containing Group III-V compound semiconductor layer (item 103) (pg. 8, paragraph [0059]; Fig. 2).

11. It would have been obvious for one of ordinary skill in the art at the time of the invention to form a pn-junction compound semiconductor light-emitting device as disclosed by Inoguchi et al. comprising a stacked structure including a conductive boron containing Group III-V compound semiconductor layer formed on the light-emitting part, and wherein the light permeable substrate is joined to the stacked structure through the boron containing Group III-V compound semiconductor layer as disclosed by Udagawa with at least the motivation of forming a semiconductor layer exhibiting excellent surface flatness and thus allow the light emitting device to exhibit high emission intensity (pg. 5, paragraph [0039], lines 14-18; pg. 10, paragraph [0074], lines 9-15).

12. Regarding claim 2, Inoguchi et al. as modified by Udagawa discloses a pn-junction compound semiconductor light-emitting device as described in regards to claim 1, wherein the conductive layer (item 103) has a bandgap at room temperature which is

greater than that of the light-emitting layer (item 104) and not exceeding 5.0 eV. (Udagawa, pg. 8, paragraphs [0059]; Figs. 2; same motivation).

13. Regarding claim 4, Inoguchi et al. discloses a pn-junction compound semiconductor light-emitting device as described in regards to claim 1.

14. Inoguchi et al. does not disclose a pn-junction compound semiconductor light-emitting device, wherein the conductive layer is composed of a Group III-V compound semiconductor containing arsenic and boron.

15. However Udagawa et al. discloses a pn-junction compound semiconductor light-emitting device, wherein the conductor layer (item 103) is composed of a Group III-V compound semiconductor containing arsenic and boron (pg. 3, paragraph [0029], lines 1-7; pg. 4, paragraph [0032]; lines 19-26; Figs. 1-2).

16. It would have been obvious for one of ordinary skill in the art at the time of the invention to form a pn-junction compound semiconductor light-emitting device as disclosed by Inoguchi et al., wherein the conductor layer is composed of a Group III-V compound semiconductor containing arsenic and boron as disclosed by Udagawa et al. thus providing a light-emitting device with improved structure having excellent electrical and emission characteristics (pg. 2, paragraph [0009])

17. Regarding claim 5, Inoguchi et al. as modified by Udagawa et al. discloses a pn-junction compound semiconductor light-emitting device as described in reference to claim 1, wherein the conductive layer (item 103) is composed of a Group III-V compound semiconductor containing phosphorus and boron (Udagawa, pg. 8, paragraphs [0059]; Figs. 2; same motivation).

18. Regarding claim 6, Inoguchi et al. as modified by Udagawa et al. discloses a pn-junction compound semiconductor light-emitting device as described in reference to claim 5, wherein the conductive layer (item 103) is composed of boron phosphide (Udagawa, pg. 8, paragraphs [0059]; Figs. 2; same motivation).

19. Regarding claim 12, Inoguchi et al. as modified by Udagawa et al. discloses a pn-junction compound semiconductor light-emitting device as described in reference to claim 1, wherein the conductive layer (item 103) has a conduction type which is the same as a conduction type of an upper clad layer (item 102) of the light emitting layer (Udagawa, pg. 8, paragraphs [0059]; Figs. 2; same motivation).

20. Regarding claim 13, Inoguchi et al. discloses a pn-junction compound semiconductor light-emitting device as described in reference to claim 1, wherein an ohmic electrode (item 45) is formed on a surface of the device opposite the light permeable substrate (item 23) (pg. 5, paragraph [0089]; Fig. 2E).

21. Claims 3 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoguchi et al. (U.S. Pub. Application 2006/0094140 A1) and further in view of Udagawa (U.S. Pub. Application 2003/0160253 A1) as applied to claim 1 above and in further in view of Udagawa (U.S. Pub. Application 2003/0160253 A1).

22. Regarding claim 3, Inoguchi et al. as modified by Udagawa discloses a pn-junction compound semiconductor light-emitting device as described in regards to claim 1.

23. Neither Inoguchi et al. nor Udagawa disclose a pn-junction compound semiconductor light-emitting device wherein the conductive layer is composed of an

undoped Group III-V compound semiconductor containing boron to which an impurity element has not been intentionally added.

24. However Udagawa et al. discloses a pn-junction compound semiconductor light-emitting device wherein the conductor layer (item 103) is composed of an undoped Group III-V compound semiconductor containing boron to which an impurity element has not been intentionally added (pg. 6, paragraphs [0043]; Figs. 2-4).

25. It would have been obvious for one of ordinary skill in the art at the time of the invention to form a pn-junction compound semiconductor light-emitting device as disclosed by Inoguchi et al. as modified by Udagawa wherein the conductive layer is composed of an undoped Group III-V compound semiconductor containing boron to which an impurity element has not been intentionally added as disclosed by Udagawa et al. with at least the reason of forming a layer with excellent surface flatness and continuity (pg. 5, paragraph [0039], lines 14-18).

26. Regarding claim 7, Inoguchi et al. as modified by Udagawa discloses a pn-junction compound semiconductor light-emitting device as described in regards to claim 1.

27. Neither Inoguchi et al. nor Udagawa disclose a pn-junction compound semiconductor light-emitting device, wherein the conductive layer is composed of a boron-containing Group III-V compound semiconductor containing twins.

28. However Udagawa et al. discloses a pn-junction compound semiconductor light-emitting device, wherein the conductive layer (item 103) is composed of a boron-containing Group III-V compound semiconductor containing twins (pg. 6, paragraph [0044]; Figs. 2-4).

29. It would have been obvious for one of ordinary skill in the art at the time of the invention to form a pn-junction compound semiconductor light-emitting device as disclosed by Inoguchi et al. as modified by Udagawa, wherein the conductive layer is composed of a boron-containing Group III-V compound semiconductor containing twins as disclosed by Udagawa et al. thus providing a device with excellent crystallinity between the conductor layer and light emitting layer (pg. 6, paragraph [0044], lines 14-18).

30. Regarding claim 8, Inoguchi et al. as modified by Udagawa et al. discloses a pn-junction compound semiconductor light-emitting device as described in reference to claim 7, wherein each of the twins has, as a twinning plane, a (111) lattice plane of a boron-containing Group III-V compound semiconductor (Udagawa, pg. 6, paragraph [0044]; Figs. 2-4; with the same motivation).

Conclusion

31. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VERNON P. WEBB whose telephone number is (571)270-3332. The examiner can normally be reached on Monday through Friday, 7:30 am to 5 pm, Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1760. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/V. Parris Webb/
Examiner, Art Unit 2811